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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/671,334 | 09/24/2003 | Yu-Tung Huang | 38699-8035US | 5674 |

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| EXAMINER | |
|---|---|
| WILLIAMS, ALEXANDER O | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/671,334 | HUANG ET AL. | |
| | Examiner | Art Unit | |
| | Alexander O. Williams | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2005 and 12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,7-9,11 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9,11 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/671334 Attorney's Docket #: 38699-8035US
Filing Date: 9/24/2003;

Applicant: Yu-Tung Huang

Examiner: Alexander Williams

Applicant's RCE/amendment filed 12/12/05 has been acknowledged.

Applicant's Amendment filed 12/9/05 to the election without of Group I (claims 1 to 21), filed 7/15/04, has been acknowledged.

Claims 5, 6, 10, and 12-21 have been canceled.

Claims 7 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "said lower surface" in claim 7. There is insufficient antecedent basis for this limitation in the claim.

Any of claim 7 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 7, 8, 9 and 22-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilleo et al. (U.S. Patent Application Publication # 2005/0056946 A1) in view of Applicant's Prior Art figures 1A-1F.

As to claim 1, Gilleo et al. (figures 1 to 5) specifically figure 5 show a package assembly for an electronic device, comprising: a substrate **7** having a first surface with a first plurality of contact pads **39**, and a buffer layer **45** between said substrate and said electronic device, and a surface of said electronic device having electrodes **27** being opposite to said first surface of said substrate, said buffer layer having an opening to expose said first plurality of contact pads, wherein said buffer layer has a first part with a first density and a second part with a second density, said first density greater than said second density, wherein said second part of said buffer layer surrounds the edge of said electronic device and said first part of said buffer layer is configured with said electronic device and said first part of said buffer layer functions as a self-planarization buffer between said electronic device and said substrate for increasing the hermeticity thereof.

Applicant Prior Art figure 1B show a package assembly for an electronic device, comprising: a substrate **220** having a first surface with a first plurality of contact pads **(shown but not labeled)** and a second plurality of contact pads **(shown but not labeled)**, a second surface with a plurality of connection pads (shown but not labeled), and a plurality of via holes (metal traces within the substrate) connecting said first plurality of contact pads and said plurality of connection pads for the purpose of providing electrical connection to external devices.

2. The package assembly in claim 1, the combination wirh Applicat's Prior Art figure 1B showing wherein the material of said substrate is selected from the group consisting a ceramic substrate, alumina substrate, a silicon substrate, a polymer substrate and a glass substrate.

3. The package assembly in claim 1, the combination with Gilleo et al. showing wherein said buffer layer is selected from the group consisting of an organic film layer and a polymer film layer (see page 2, paragraph [0021]).

7. The package assembly in claim 1, the combination with Applicant's Prior Art figure1F show where a conductive layer is formed on said electronic device with respect to said lower surface.

8 and 18. The package assembly in claim 1 or 12, Gilleo et al. show wherein said first part has a relatively greater thickness and said second part has a relatively smaller thickness between 30-200 microns. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

9. The package assembly in claim 1, Gilleo et al. show wherein said first part is higher than said lower surface of said electronic device in altitude, contacted closely with said electronic device and disposed horizonally outside said electronic device.

11. The package assembly in claim 12, Gilleo et al. show wherein said fastening faces of said edge of said plurality of electronic devices and said buffer layer have a corner respectively.

22. Gilleo et al. (figures 1 to 5) specifically figure 5 show a package assembly for an electronic device **3** having a lower surface having electrodes **27** thereon, an upper surface and a vertical side with respect to said lower surface, comprising: a substrate **7** having a first surface with a first plurality of contact pads **39**; a buffer layer **45** disposed on said substrate and having an opening to expose said first plurality of contact pads, wherein said buffer layer further has a first part and a second part, said first part being lower than said upper surface of said electronic device and higher than said lower surface of said electronic device in altitude.

Applicant Prior Art figure 1B show a package assembly for an electronic device, comprising: a substrate **220** having a first surface with a first plurality of contact pads **(shown but not labeled)** and a second plurality of contact pads **(shown but not labeled)**, a second surface with a plurality of connection pads (shown but not labeled), and a plurality of via holes (metal traces within the substrate) connecting said first plurality of contact pads and said plurality of connection pads for the purpose of providing electrical connection to external devices.

23. Gilleo et al. (figures 1 to 5) specifically figure 5 show a package assembly for an electronic device **3** having a lower surface having electrodes **27** thereon, an upper surface and a vertical side with respect to said lower surface, comprising: a substrate **7** having a first surface with a first plurality of contact pads **39**; and a buffer layer **45**

disposed substantially between said substrate and said electronic device and having an opening to expose said first plurality of contact pads, wherein said buffer layer further forms a shoulder with a first surface disposed alongside said vertical side of said electronic device and being contacted closely with said vertical side and a second surface bearing said electronic device at said lower surface and being contacted closely with said lower surface.

Applicant Prior Art figure 1B show a package assembly for an electronic device, comprising: a substrate **220** having a first surface with a first plurality of contact pads **(shown but not labeled)** and a second plurality of contact pads **(shown but not labeled)**, a second surface with a plurality of connection pads (shown but not labeled), and a plurality of via holes (metal traces within the substrate) connecting said first plurality of contact pads and said plurality of connection pads for the purpose of providing electrical connection to external devices.

24. The package assembly for an electronic device according to claim 23, the combination with Gilleo et al. showing wherein said first surface being higher than said second surface in altitude and integrally formed with each other.

25. Gilleo et al. (figures 1 to 5) specifically figure 5 show a package assembly for an electronic device **3** having a lower surface having electrodes **27** thereon, an upper surface and a vertical side with respect to said lower surface, comprising: a substrate **7** having a first surface with a first plurality of contact pads **39**; and a buffering means **45** and a hermetical sealing means formed integrally, disposed substantially between said substrate and said electronic device and being contacted with a corner of said electronic device associated with said lower surface, wherein said hermetical sealing means is further contacted closely with said vertical side and said buffering means is further contacted closely with said lower surface.

Applicant Prior Art figure 1B show a package assembly for an electronic device, comprising: a substrate **220** having a first surface with a first plurality of contact pads **(shown but not labeled)** and a second plurality of contact pads **(shown but not labeled)**, a second surface with a plurality of connection pads (shown but not labeled),

and a plurality of via holes (metal traces within the substrate) connecting said first plurality of contact pads and said plurality of connection pads for the purpose of providing electrical connection to external devices.

26. Gilleo et al. (figures 1 to 5) specifically figure 5 show a package assembly for an electronic device **3** having a lower surface having electrodes **27** thereon, comprising: a substrate **7** having a first surface with a first plurality of contact pads **39**; and a buffer layer **45** disposed substantially between said substrate and said lower surface of said electronic device and having an opening to expose said first plurality of contact pads, wherein said buffer layer has a first part with a first density and a second part with a second density greater than said first density.

Applicant Prior Art figure 1B show a package assembly for an electronic device, comprising: a substrate **220** having a first surface with a first plurality of contact pads **(shown but not labeled)** and a second plurality of contact pads **(shown but not labeled)**, a second surface with a plurality of connection pads (shown but not labeled), and a plurality of via holes (metal traces within the substrate) connecting said first plurality of contact pads and said plurality of connection pads for the purpose of providing electrical connection to external devices.

Therefore, it would have been obvious to one of ordinary skill in the art to use the teaching of Applicant's Prior Art figure 1B substrate to modify Gilleo et al.'s device substrate for the purpose of providing electrical connection to external devices.

Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilleo et al. (U.S. Patent Application Publication # 2005/0056946 A1) in view of Applicant's Prior Art figure 1B and further in view of Fukihura (U.S. Patent # 5,150,748).

The combination show the claimed invention as detailed above, but fail to explicitly show wherein said electronic device is a surface acoustic wave device

Fukiharu is cited for showing a surface acoustic wave device. Specifically, Fukiharu (figures 1 and 2) discloses a package assembly for an electronic device, comprising: a substrate **11** having a first surface with a first plurality of contact pads **4-1** and a second plurality of contact pads **4-2;** a second surface with a plurality of connection pads **10-1,10-2**, and a plurality of via holes **9-2,9-1** connecting said first plurality of contact pads and said plurality of connection pads; a second surface with a plurality of connection pads, and a plurality of via holes connecting said first plurality of contact pads and said plurality of connection pads and wherein said electronic device is a surface acoustic wave device **1** for the purpose of being capable of electrically shielding the SAW element against an external electric field while design to have a small volume.

11. The package assembly in claim 1, the combination with Fukiharu (figure 5) show wherein said electronic device is a surface acoustic wave device **1**.

Therefore, it would have been obvious to one of ordinary skill in the art to use the teaching of Fukihura's SAW device for the combination device for the purpose of being capable of electrically shielding the SAW element against an external electric field while design to have a small volume.

# Response

Applicant's arguments filed 12/9/05 have been fully considered, but are moot in view of the modified grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/778,680,774,772,779,737,734,738,690,691,696,698,6<br>68,787,784,786,700,701,758,783<br>310/348,313 R,340,344<br>174/260,261<br>361/760,772,777<br>385/14,49,91<br>333/133,193 | 9/13/04<br>4/8/05<br>9/15/05 |
| Other Documentation:<br>foreign patents and literature in<br>257/778,680,774,772,779,737,734,738,690,691,696,698,6<br>68,787,784,786,700,701,758,783<br>310/348,313 R,340,344<br>174/260,261<br>361/760,772,777<br>385/14,49,91<br>333/133,193 | 9/14/04<br>4/8/05<br>9/15/05 |
| Electronic data base(s):<br>U.S. Patents EAST | 9/14/04<br>4/8/05<br>9/15/05 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
1/9/06

Primary Patent Examiner
Alexander O. Williams